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# Monolithic integration of Si nanowires with metallic electrodes: NEMS resonator and switch applications

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### Abstract

The challenge of wafer-scale integration of silicon nanowires into microsystems is addressed by developing a fabrication approach that utilizes a combination of Bosch-process-based nanowire fabrication with surface micromachining and chemical-mechanical-polishing-based metal electrode/contact formation. Nanowires up to a length of 50  $\mu$ m are achieved while retaining submicron nanowire-to-electrode gaps. The scalability of the technique is demonstrated through using no patterning method other than optical lithography on conventional SOI substrates. Structural integrity of double-clamped nanowires is evaluated through a three-point bending test, where good clamping quality and fracture strengths approaching the theoretical strength of the material are observed. Resulting devices are characterized in resonator and switch applications-two areas of interest for CMOS-compatible solutions—with all-electrical actuation and readout schemes. Improvements and tuning of obtained performance parameters such as resonance frequency, quality factor and pull-in voltage are simply a question of conventional design and process adjustments. Implications of the proposed technique are far-reaching including system-level integration of either single-nanowire devices within thick Si layers or nanowire arrays perpendicular to the plane of the substrate.

(Some figures in this article are in colour only in the electronic version)

# 1. Introduction

Recently, there have been intense research efforts in nanoelectronics and nanoelectromechanical systems (NEMS) for resonator and switch applications. In this respect, Si nanowires (SiNWs) are known to impart valuable capabilities to existing systems thanks to a variety of interesting physical properties including giant piezoresistivity due to electron and hole trapping [1], fracture strengths approaching the theoretical strength of crystalline Si [2] and ultra-high resonance frequencies on the order of hundreds of MHz [3]. Their uses within nanoelectronics and NEMS are especially appealing due to their compatibility with existing process technologies. This compatibility raises the possibility of

batch processing and hence constitutes a major advantage for system-level integration.

SiNWs were investigated as resonators beginning from the late nineties for gravimetric sensing applications [4]. With the advances in fabrication methods, the size of SiNWs reached below 10 nm [5–7]. Using different measurement methods, the resonance of SiNWs ranging from 400 kHz [8] to about 400 MHz [9] was measured. Quality factors up to 25 000 [5] were achieved in vacuum, whereas in air, quality factors ranged between 150 [10] and 400 [11]. SiNWs were brought to resonance either electrostatically [4, 8–10, 12, 13], magnetomotively [3, 14, 15], by thermal excitation [11] or by the use of base excitation via a piezoelectric stage [5, 16–19]. Optical interference [4, 5, 9–11, 17] or capacitive [12, 13], magnetomotive [3, 15] and piezoresistive [18, 20] readout techniques were employed for resonance detection.

Compared to resonator applications, the use of SiNWs as electromechanical switches was demonstrated more recently [21]. Although carbon nanotubes (CNTs) form the main class of nanostructures used in electromechanical switch application [22–24], their synthesis generates both metallic and semiconducting CNTs rendering CNT-based NEMS difficult to predict. In contrast, with the possibility of tailoring both their electronic properties and critical dimensions during growth, SiNWs provide reliable switch behavior [25]. Such switches were originally fabricated by clamping SiNWs near a metal electrode and measuring the pull-in voltage [25–27]. Resultant devices had no power consumption at the off-state and exhibited an on/off current gain of 10<sup>4</sup>.

In device applications—similar to those mentioned above—a deterministic assembly is highly preferable. Integration of SiNWs with higher order structures constitutes the most critical step for the functionality of NEMS as many nanofabrication techniques are not compatible with photolithography.

In vapor-liquid-solid (VLS) synthesis, one of the most widely used bottom-up techniques for SiNW fabrication, two major approaches for integration are available. VLS results in well-controlled diameter and crystallographic orientation, which is  $\langle 1 \ 1 \ 1 \rangle$  for SiNWs with a diameter larger than 20 nm and  $\langle 1 \ 1 \ 0 \rangle$  for SiNWs with a diameter lower than 10 nm [28]. The main integration approach for VLS products is to disperse synthesized NWs in a solvent, where they are subsequently directed into alignment. Alignment can be achieved by applying external electric or magnetic fields or inducing a microfluidic flow over the dispersed SiNWs. These methods require lengthy and complex procedures with limited yield. There are reported applications of such an approach to fabrication of SiNW resonators [19]. In the alternative method, SiNWs are synthesized on the spot of interest. This necessitates selective placement of catalytic Au particles through a nanolithographic technique. The yield is much better than that achieved through external alignment, and hence, most of the device demonstrations utilize this onsite growth technique [3, 5, 15, 17, 18]. In addition to proper patterning, subsequent fabrication of excitation and read-out components brings about its own set of challenges including material selectivity for various deposition and etching steps.

Integration can also take place through a top-down technique. The most direct approach is placement of NWs with a manipulator. Its complexity resembles direct-write techniques such as e-beam-induced deposition or focused ion beam milling. This method was employed in the fabrication of SiNW resonators in [8] and SiNW switches in [21, 26, 27].

Alternatively, a nanolithographic technique can be used either as a positive process where anisotropic etching defines a SiNW beneath a mask or as a negative process where a trench is used as a mold for the subsequent deposition of a nanowire. The latter technique is more applicable in the case of polycrystalline metallic NWs deposited through electroplating, whereas the former technique requires a very thin device layer such as the single crystalline SiC film used in a



Figure 1. Different approaches to single-crystalline SiNW formation using top-down patterning and etching.

resonator study [29]. Various reported works are also available on SiNW resonators using this approach [4, 9–14, 16, 20]. For single crystalline Si, a similar approach is possible with SIMOX wafers with a very thin Si layer on buried oxide [30]. Further reduction in size can be achieved through oxidation [31]. Working with much thicker Si layers is also possible when one uses the scalloping effect of the Bosch process in inductively coupled plasma deep reactive ion etching (ICP-DRIE). In this technique, one takes advantage of the undercuts created by the isotropic etch step [32]. This technique also raises the possibility of fabricating a vertical array of SiNWs. A comparison of these techniques is provided in figure 1. As opposed to the bottom-up approach to SiNW integration, such top-down techniques inherently possess a higher potential for system integration.

Scalloping, seen in the third column in figure 1, is a well-known phenomenon encountered in the Bosch process in ICP-DRIE, where the chemical etch step leads to small undercuts on side walls. The extent of this undercut is a direct indication of chemical etch parameters such as etch duration. Hence, by adjusting chemical etch parameters one can change scallop geometry. If one etches a thin column (around 1  $\mu$ m thickness) from both sides via the Bosch process in ICP-DRIE, the scallop geometry can be adjusted to consume Si until the scallops meet and form a single SiNW whose diameter can be further decreased through oxidation [33-38]. In similar studies, oxidation is shown to act as a modifier of the SiNWs, and pentagonal [36-39], triangular [34, 35, 37] and circular cross-sections [33] can be obtained. Most of these studies are based on isotropic etching with a pronounced undercut effect. In addition, a vertical array of Si strings can be achieved with the Bosch process. By further oxidation and sacrificial etch, a stack of SiNWs can be obtained as a result. This technique is



Figure 2. SEM image of the device.

unparalleled in its ease of producing vertical SiNW stacks as well as a single SiNW in a thick Si device layer.

The technique based on the Bosch process was first introduced by Milanovic et al [32] in an effort to fabricate lateral field emission devices. Doherty et al investigated the relationship between the SiNW diameter and the photoresist width and fabricated nanochannels utilizing ICP-DRIE [40]. Ng et al further investigated the effect of oxidation on the eccentricity of the formed SiNWs and suggested that eccentricity decreases as oxidation time increases [41]. Following this research, Ng et al employed this method to form vertically stacked SiNW transistors [42]. Supplementary to these studies, Ozsun et al investigated the aspect ratio and depth limits of this method and the mechanical integrity of fabricated SiNWs [43]. In addition, patterns other than straight SiNWs and integration of SiNWs with microsystems or MEMS such as microtweezers were demonstrated. Bopp et al presented an additional process flow to fabricate separated vertical stacks of SiNWs [44].

In this work, the technique based on the Bosch process is used to produce a single SiNW within a thick Si device layer to demonstrate suitability for system integration in nanomechanical resonator and switch applications. In such applications, if integration with electronics is targeted, electrostatic actuation and capacitive readout are necessary, as optical or magnetic means are incompatible with the associated systems' requirements. This raises the need for metallic components, as they reduce loss throughout the device due to their low resistance and serve as high-performance electrodes both for actuation and readout, base grounding and shielding components. Hence, metal elements-aluminum in this case-should be incorporated into the design to ensure high-quality performance and ease the integration to more complicated CMOS circuits.

For this purpose, the ICP-DRIE technique is extended in a unique way to incorporate metallic elements as actuation and readout electrodes. The major claim of the work is the enhancement of CMOS integration for future, NEMSbased, on-chip components. Surface micromachining with a combination of conventional photolithography and selfaligned masking through chemical–mechanical polishing (CMP) is utilized, reducing the overall complexity of the process. Instead of a single SiNW, the fabrication method is also adjustable for the fabrication of SiNW stacks between metallic electrodes. In the remainder of this paper, the architecture of the device and instrumentation are introduced first followed by the fabrication of the devices. Nanoelectromechanical resonator and switch applications are demonstrated next. The mechanical behavior and structural reliability of the proposed system are also characterized using a three-point bending test.

# 2. System architecture and instrumentation

The chosen architecture for the device is a single SiNW suspended in a doubly clamped fashion between two Al electrodes as seen in figure 2. Al electrodes are of 1.5  $\mu$ m thickness and reside on the buried oxide (BOX) layer of the SOI wafer on which the device is fabricated. Fabricated SiNWs are along the  $\langle 1 0 0 \rangle$  orientation and have a length of 50  $\mu$ m and diameters of 50–200 nm. Al electrodes extend throughout the whole length of SiNWs with a gap of 900 nm on both sides.

# 2.1. Nanoelectromechanical resonator geometry and instrumentation

Electrostatic actuation and capacitive readout are commonly employed in nanoelectromechanical resonators [3]. A similar approach is utilized here to characterize fabricated SiNW– electode assembly as a resonator. An HP 8753 D network analyzer is used to actuate and carry out transmission measurement as depicted in figure 3. An amplifier is placed between the network analyzer and the readout electrode. Measurements are carried out in a Cascade probe station. The amplitude of the ac voltage,  $V_{ac}$ , applied to the actuation electrode is kept at 40 mV. Six sets of experiments are carried out by increasing the dc bias,  $V_{dc}$ , applied to the Si pads from 0 to 70 V. In each set of experiments, a frequency sweep is conducted to detect resonance.

This readout geometry tracks the motional current as a result of capacitive changes between the SiNW and the readout electrode as the SiNW is at resonance. On the other hand, there exists a large parasitic capacitance between the electrodes that dominates the measurements. Finite-element simulations of the device estimate a parasitic capacitance of 18 fF. It is due to this large parasitic effect that measurements obtained from the network analyzer cannot directly demonstrate the resonance of SiNWs. To remove the parasitic current from measurements, the following formulation is needed.



Figure 3. Schematic setup for resonator application.

The total current, I, obtained from the readout electrode can be written as

$$I = I_p + I_m \cong C_p \frac{\partial V_{ac}}{\partial t} + (V_{dc} + V_{ac}) \frac{\partial \Delta C}{\partial t}, \qquad (1)$$

where  $I_p$  is the parasitic current,  $I_m$  is the motional current,  $C_p$  is the parasitic capacitance and  $\Delta C$  is the capacitance difference due to SiNW vibration. In the absence of  $V_{dc}$ , the resultant current can be written as

$$I = I_p + I_m \cong C_p \frac{\partial V_{\rm ac}}{\partial t} + V_{\rm ac} \frac{\partial \Delta C}{\partial t}.$$
 (2)

Since  $\Delta C \ll C_p$ , the term given in equation (2) becomes equal to the parasitic current. As a result, the current measured when the SiNW is grounded can be taken as the parasitic current. Furthermore, when  $V_{\rm dc} \gg V_{\rm ac}$ , the resultant current can be simplified as

$$I = I_p + I_m \cong C_p \frac{\partial V_{\rm ac}}{\partial t} + V_{\rm dc} \frac{\partial \Delta C}{\partial t}.$$
 (3)

Therefore, to eliminate the parasitic current from measurements, the measurement taken at zero  $V_{dc}$ (equation (2)) should be subtracted from the data obtained at a given  $V_{dc}$  (equation (3)).

Resonance frequency is a function of the stiffness of SiNWs, which derives from both the elasticity of silicon crystal and its internal stress. Previous studies suggest that a SiNW above 100 nm critical dimension should exhibit modulus of elasticity of bulk Si as summarized in [45]. Hence, any variation in our study from analytical predictions will be taken to be a result of intrinsic stresses, which can be formulated as given in equation (4) [46]:

$$\omega = \frac{\beta^2}{2l^2} \left(\frac{EI}{\rho A}\right)^{1/2} \sqrt{1 + \frac{2l^2}{7h^2}\varepsilon_s}.$$
 (4)

Here,  $\omega$  is the resonance frequency,  $\varepsilon_s$  is the longitudinal strain due to intrinsic stress,  $\beta = 4.73$  is the first mode shape parameter, *l* is the length, *h* is the thickness, *I* is the moment of inertia, A is the cross-sectional area,  $\rho$  is the density and E is the modulus of elasticity of the SiNW. Using this formulation, the effect of internal stress can be quantified.

### 2.2. Nanoelectromechanical switch geometry and instrumentation

As well as the resonator application, utilized geometry also provides a suitable platform for switch applications. As the



Figure 4. Schematic of the switch application setup. -40 V was applied from port A and the voltage applied by port B was swept from -40 to 40 V. The current between the ports C and D was measured. The inset is an optical micrograph of a SiNW after pull-in. Green and red fringes, an indication that the diameter is below the minimum wavelength of visible light, are observed along this bent SiNW, whose position and size shift with increasing deformation.

voltage difference between the SiNW and a nearby electrode is increased, SiNW deflects toward the electrode until pull-in occurs and the SiNW attaches itself to the electrode. Pull-in manifests itself as a jump in the current between the SiNW and the read-out electrode. The schematic of the setup can be seen in figure 4. Here devices are placed in a Cascade probe station with the probes connected to an HP 4156A semiconductor parameter analyzer (SPA). A dc voltage of -40 V is applied to the Si pads and one electrode, whereas a dc voltage varying from -40 to 40 V is applied to the counter electrode. As the voltage difference is increased, the current between the ports C and D is monitored.

The pull-in voltage,  $V_{\rm PI}$ , can be calculated analytically by the following formula [47]:

$$V_{\rm PI} = \sqrt{\frac{8K_{\rm eff}d_0^3}{20.9\varepsilon_0 lb_{\rm eff}}},\tag{5}$$

where  $K_{\text{eff}}$  is the effective stiffness of the resonator,  $d_0$  is the zero-voltage gap between the SiNW and the read-out electrode,  $\varepsilon_0$  is the permittivity of free space and  $b_{\rm eff}$  is the effective thickness. For the device geometry of interest, the effective stiffness formula of a string can be used as seen in equation (6):

$$K_{\rm eff} = \frac{32Ebh^3}{l^3} + \frac{8N}{l},$$
 (6)

where b is the width of the SiNW and N is the axial force on the SiNW. The axial force is composed of the intrinsic stress



**Figure 5.** Fabrication flow of the device. (*a*) Hard mask definition. (*b*) ICP-DRIE. (*c*) Oxidation. (*d*) Metal coating. (*e*) PR coating. (*f*) CMP. (*g*) Al etch. (*h*) Oxide etch.

as indicated by  $\varepsilon_s$  in equation (4) and axial stress due to large deformations.

#### 3. Fabrication

Fabrication is carried out on a 4" SOI wafer with a  $\langle 1 \ 0 \ 0 \rangle$ oriented and 1.5  $\mu$ m thick device Si layer and 2  $\mu$ m thick BOX. First, using LPCVD, the SOI wafer is coated with a 100 nm thick SiO<sub>2</sub> layer. This layer is then patterned by optical lithography. A 2  $\mu$ m thick positive AZ92XX photoresist is used to define two-terminal devices with a NW line residing between them. SiNW is later to be formed underneath this mask. Hence, the width of the line (1.2  $\mu$ m) is crucial for the success of the process. After the mask is defined, exposed SiO<sub>2</sub> is etched in RIE and the hard mask for the subsequent Bosch process is thus formed (figure 5(*a*)). Based on optical lithography, this step is where batch compatibility of the whole integration process is introduced and scalability is secured.

Formation of oxide hard mask is followed by the Bosch process in ICP-DRIE to form scalloped walls on trenches underneath the NW line (figure 5(*b*)). 1.5  $\mu$ m thick device Si is etched all the way to the BOX layer. Scallop size can be controlled by relative timing of the isotropic etch phase with SF<sub>6</sub> gas. With the specific recipe, scallops are formed to have radii of approximately 200 nm. In each etch cycle, 6 s of SF<sub>6</sub> and 2 s of C<sub>4</sub>F<sub>8</sub> exposure are carried out. Under these conditions, it takes four etch cycles to etch 1.5  $\mu$ m thick Si and reach BOX.

A subsequent wet oxidation step allows consumption of Si on trench walls. As a result of careful oxide growth, the Si column can be separated into Si strings enveloped within SiO<sub>2</sub>. The thickness of the grown oxide is crucial, as under-oxidation may result in failure of the release of SiNWs, whereas overoxidation may result in total consumption of the Si wall. To obtain a single SiNW, the hard mask is used as an inhibitor to SiO<sub>2</sub> growth (thus Si consumption) on the upper Si surface and oxidation is carried out until the Si wall is consumed almost entirely throughout its width (figure 5(c)). In this specific case, a wet oxidation of 820 nm at 1050 °C is observed to work well. This process can also be adjusted such that multiple SiNWs are fabricated along the scallops as shown by Ozsun *et al* [43]. In addition to shaping of SiNWs, grown oxide also serves as a protective layer in subsequent harsh treatments and defines the SiNW-electrode gap. It is this step where a uniform and submicron SiNW-electrode gap is defined over a span of 50 µm.

Following oxidation, a 1.5  $\mu$ m thick Al film is blanketdeposited through sputtering to fill the trenches on both sides of the already oxidized NW line (figure 5(*d*)). Deposition is followed by spin-coating of a 2  $\mu$ m thick positive AZ\_ECItype resist (figure 5(*e*)). This process will lead to a self-aligned mask needed for the formation of read-out and actuation electrodes. To form a self-aligned mask, the CMP method is employed. Planarization of the surface is achieved through removing PR from the upper parts until Al layer is exposed (figure 5(*f*)). Direct CMP of Al proves to be a difficult task. Aside from being a relatively hard material, scale differences among Al portions to be removed play a detrimental role. Hence, the current process based on photoresist removal instead of Al is developed.

Subsequently, Al is wet etched until the SiO<sub>2</sub> layer is exposed (figure 5(g)). Finally, both SiO<sub>2</sub> coating surrounding the buried Si string cores and BOX layer are etched until SiNWs are released (figure 5(h)). Etching is carried out in Al-selective Silox. As a direct result of the oxide protective layer, no short between electrodes and SiNW is of concern. Furthermore, submicron SiNW–electrode gaps can be preserved over large distances.

## 4. Results and discussion

It is to be noted that in this work relatively long SiNWs (50  $\mu$ m) are fabricated to achieve resonance frequencies on the order of 1 MHz. Keeping the resonance frequency at that level facilitates addressing of rather complicated issues in actuation and readout. For the same reason, the behavior of a single SiNW will be studied instead of an array of SiNWs as



**Figure 6.** (*a*) Direct results obtained from the network analyzer for different  $V_{dc}$ . (*b*) Differential signal readout indicating net motional/dynamic current. The inset provides a close-up view of the obtained peak indicating strong dependence of the obtained signal on SiNW bias.

previously demonstrated [43]. To achieve higher frequencies and to inquire into SiNW array behavior, one can easily adjust layout and process parameters.

This section starts with the characterization of the device as a resonator followed by the demonstration of the switch behavior. The pull-in and pull-off conditions are discussed, and the suitability of the device as a high-voltage switch is investigated. The intrinsic stress in Si is computed in both cases. Finally, the results of a three-point bending test are discussed in relation to the clamping quality and the fracture strength of SiNWs.



**Figure 7.** (*a*) Effect of incident white light on the magnitude of current jump upon pull-in. (*b*) Hysteretic behavior of the switch.

#### 4.1. Resonator characterization

Figure 6(a) provides frequency sweep data from transmission measurements taken with the setup depicted in figure 3. Six different bias voltages,  $V_{dc}$ , from 0 to 70 V are used. These direct results do not yield any meaningful peaks as they indicate various interference sources irrespective of the motion of SiNW. However, when the differential signal, i.e. the difference from the results obtained with grounded SiNW, is plotted, a clear trend for the motional current is obtained. The signal is observed to strongly depend on the applied dc bias on SiNW as seen in figure 6(b). The inset shows more clearly the increasing signal, and also a close look reveals the onset of nonlinearity with increasing bias.

The resonance peak is observed at 1.97 MHz. Using equation (4), the intrinsic strain and stress can be computed. As a result, a tensile intrinsic stress of 2.8 MPa is found within the SiNW. By fitting Lorenztian curves to the measured data, the quality factor can also be calculated. Excluding the data series in which nonlinear resonance due to the hardening is observed, an average quality factor of 75 is obtained. This rather low quality factor can be attributed to the relatively low intrinsic stress present in the SOI device layer.



**Figure 8.** Scanning electron micrographs of a loading sequence in three-point bending configuration. In three-point bending samples, Al electrodes are etched deliberately to provide space for probe motion and SiNW bending deflection.

#### 4.2. Switch characterization

When the current is measured over the ports C and D in figure 4, a clear indication of pull-in of SiNWs is obtained. A graph of current versus voltage difference between the electrode and the SiNW is provided in figure 7. Current jump is due to the contact of the SiNW with the electrode upon pull-in. Measurements in the dark indicate a change in current from a few hundred fA to 1 pA resulting in an on/off current gain of 10 (lower curve in figure 7(a)). The measured few hundred fA is the minimum measurable current by the SPA. The increase in the current before pull-in is due to the tunneling of electrons. After pull-in occurs, a contact between the SiNW and the Al electrode is established in the form of a Schottky barrier. Hence, in the presence of incident white light, the magnitude of the current jump at pull-in increases three orders of magnitude (from 0.1 to 100 pA) (upper curve in figure 7(a)). Pull-in is observed at relatively high voltage differences that can be decreased by decreasing the SiNW radius or SiNW-toelectrode gap. The pull-in voltage and magnitude of the current jump remain independent of the voltage sweep parameters such as the utilized step size.

Using equations (5) and (6), the intrinsic stress within the SiNW can be computed once again. For pull-in samples, a voltage of 35 V corresponds to an intrinsic stress of 29 MPa. Although this value is ten times higher than the intrinsic stress of 2.8 MPa computed on resonance samples, it is still too low for any practical purpose. This deviation is thought to be a result of minor cross-sectional changes encountered over the large span of 50  $\mu$ m, which is considered in none of the analytical formulations of equations (4)–(6).

As the voltage difference is decreased after pull-in, the SiNW stays attached to the Al electrode until its release takes place at a lower voltage level leading to hysteretic behavior as indicated by the arrows in figure 7(b). Prior to the release, the contact area between the SiNW and the Al electrode decreases gradually. Therefore, the measured current is a few tens of pA when the release occurs. Since the maximum current attained remains below 1 nA, no damage to the SiNW or the Al electrodes is observed as reflected by the hysteretic behavior of measured current. Hence, the measured pull-in voltage exhibits consistency in consecutive experiment sets.

# 4.3. Three-point bending results

To evaluate the strength of clamping, which plays an important role in both resonance and pull-in behavior, a threepoint bending test is conducted within a scanning electron microscope. The experiment provides information on the fracture strength of SiNW in case the failure does not take place at the clamps. A sharp tungsten probe (500 nm radius of curvature) driven by a micro-manipulator (miBot by Imina Technologies) is used for this purpose. Al electrodes are removed by etching to provide space for the bending test. With the tungsten tip, SiNWs are loaded at their mid-span until fracture. The deformation of SiNWs is observed and measured through scanning electron micrographs. The fracture strength is extracted from these data by large-deformation modeling.

Steps from a sample test are provided in figure 8. Fracture takes place in all tests at the mid-point denoting the high quality of the clamping. Carved from the same crystal, the SiNW and the supports are not joined through an interface. This provides an ideal setup for the measurement of fracture strength, as failure at the support is eliminated. An average deflection of 5.9  $\mu$ m is recorded at fracture. This is almost 30 times their diameter. The last micrograph in figure 8 is very close to the onset of fracture.

Large-displacement finite element analysis with bulk Si modulus of elasticity and intrinsic stress calculated from the resonator characterization is used. COMSOL software is employed in this analysis with 637 Lagrange-cubic triangular elements corresponding to 3420 degrees of freedom. The external load is distributed at the mid-span of SiNW over a length of 300 nm. The stress corresponding to a mid-span deflection of 5.9  $\mu$ m is computed. The inset in figure 8 shows the stress distribution in the vicinity of the point of contact. The resulting fracture strength is thus computed to be 14 GPa. This value is close to one-tenth of the modulus of elasticity of Si, a good approximation of the theoretical strength [2].

#### 5. Conclusion

Large-scale integration of nanostructures into microsystems raises considerable challenges in today's technology. The major challenge is parallel or wafer-scale processing that requires fabrication of micro- and nanoscale structures without any interruption of the batch by a serial technique. Leading to low cost and high throughput, the resulting scalability forms the ultimate criterion of success in the transition from pilot to batch fabrication. In this work, a fabrication process is proposed for the integration of a single SiNW or an array of SiNWs with microscale metallic electrodes/contacts. The use of optical lithography along with the Bosch process on simple SOI wafers ensures batch compatibility. For the definition of metal electrodes, a unique CMP procedure is developed leading to the formation of self-aligned masking. All processes are CMOS-compatible.

The demonstration of the resulting SiNW–Al electrode pairs as resonators and switches is carried out. All actuation and read-out steps are conducted electrically to highlight the suitability of the proposed device for fully electronic, onchip solutions. The resonance frequency of 1.97 MHz with a quality factor 75 is measured. Repeatable and hysteretic pullin and pull-out behavior is found in a range of 30–40 V, which can be further decreased by decreasing the SiNW–electrode gap or SiNW radius. The structural integrity of SiNWs is also tested through a three-point bending test, where fracture strengths approaching the theoretical strength of the material are observed. No failure at clamping points is encountered.

The length of all SiNW samples is kept at 50  $\mu$ m leading to slenderness ratios (SiNW length-to-diameter ratio) on the order of 500 and relatively low resonance frequencies. Besides demonstrating the capability of the proposed fabrication technique to yield SiNWs of very high slenderness ratios, another reason behind this choice is the intention to limit resonance frequencies to around 1 MHz. Avoiding higher frequencies helps address already complicated issues related to electrostatic actuation and capacitive readout. There is much more room for miniaturization to achieve higher frequencies, which can be realized through SiNW length reduction through optical lithography. Increasing intrinsic stress through doping or oxidation is also found to be a viable option to improve relatively low quality factors. Similarly, an electrode-to-SiNW gap of 900 nm is preserved. Pull-in voltages can further be reduced by reducing either this gap size through the amount of sacrificial oxidation prior to the release step or SiNW diameter. The extension of the work to an array operation instead of a single SiNW is currently under study.

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