Received 08 June 2015; revised 16 July 2015; accepted 17 July 2015. Date of publication 30 November 2015.
The review of this paper was arranged by Associate Editor Franz Kreupl.

Digital Object Identifier 10.1109/XNANO.2015.2469312

Monolithic Fabrication of Silicon Nanowires Bridging Thick Silicon Structures

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This work was supported in part by Tubitak under Grant 112E058 and in part by the Koç University–Istanbul Rotary Club Fundamental Research Seed Fund Program. The work of Z. Tasdemir was supported by the Swiss Government Excellence Scholarship. The work of G. Fantner was supported in part by the European Union FP7/2007-2013/ERC under Grant 307338-NaMic and in part by the Swiss National Science Foundation under Grant 205320_152675.

ABSTRACT A monolithic process is developed for the fabrication of Si nanowires within thick Si substrates. A combination of anisotropic etch and sidewall passivation is utilized to protect and release Si lines during the subsequent deep etch. An etch depth of 10 μm is demonstrated with a future prospect for 50 μm opening up new possibilities for the deterministic integration of nanowires with microsystems. Nanowires with in-plane dimensions as low as 20 nm and aspect ratios up to 150 are obtained. Nanomechanical characterization through bending tests further confirms structural integrity of the connection between nanowires and anchoring Si microstructures.

INDEX TERMS Atomic force microscopy (AFM), bending test, silicon nanowires, single crystal reactive etching and metallization (SCREAM).

I. INTRODUCTION

One-dimensional nanostructures have gained a considerable attention in the field of semiconductor technology [1]. With the help of rapid development in the process technology, further miniaturization opened the gate to devices with new capabilities [2]–[4]. One such area of interest is the integration of one-dimensional nanostructures, such as nanowires (NWs), with microelectromechanical systems (MEMS), where the addition of the nanoscale element brings up enhanced functionality [5] as exemplified by the improved measurement resolution thanks to the combination of Si NWs with microscale shuttles in inertial MEMS sensors [6].

Combination of two entities, Si NW and MEMS, with a three-order of magnitude scale difference is difficult to carry out within the boundaries of the monolithic process. There are, of course, various alternatives including directional etching [7] or the possibility of growing Si NWs via vapor-liquid-solid (VLS) [8] and chemical vapor deposition [9] after MEMS fabrication. However, none of these techniques have been able to meet the stringent requirements of batch fabrication so far. An exception is the top-down approach, where Si NWs are fabricated within the thin device layer (250 nm) of a silicon on insulator (SOI) wafer, on top of which a thick (10 μm) poly-Si is deposited for MEMS fabrication [6]. The need for thin SOI and use of multiple Si layers increases demands on the already challenging fabrication process. Nevertheless, advantages of Si NW integration justify this extra effort. This approach already raised new opportunities in the miniaturization of multiple degree-of-freedom inertial sensors [10].

In this work we explore the limits of batch fabricating a single NW within a thick Si layer with two objectives that go beyond the state of the art [6]. The Si NW is to be i) fabricated within the same crystal as MEMS - as opposed to a separate Si layer, and ii) kept at the wafer surface for the ease of further processing, such as doping and contact formation.

II. PROCESS DEVELOPMENT

To achieve this set of objectives, we revisit SCREAM (Single Crystal Reactive Etching and Metallization) process [11] that played an important role in the surface micromachining of electrostatic devices. The backbone of SCREAM was a critical sidewall passivation, which would provide protection

during isotropic release etch. Similarly, if one can define a nanoscale Si line protected with a conformal sidewall coating, one can, in principle, etch deep into the substrate transforming the protected line into a Si NW. How deep one can etch the substrate while preserving the integrity of the Si NW constitutes the major motivation of this work.

The process begins with the definition of 200-nm-thick e-beam resist HSQ (Hydrogen silsesquioxane) lines on a <100> Si wafer. Linewidths between 20-80 nm are patterned parallel to <110> (Fig. 1.a). This dimension directly translates into the Si NW width (in-plane dimension). HSQ is used as an etch mask for the subsequent Cl_2 reactive ion etching (RIE) process. The etch depth is kept at 150 nm leading to the formation of Si lines (Fig. 1.b). An 80-nm thick conformal coating of low-temperature oxide (LTO) is used for sidewall protection (Fig. 1.c), which is then etched from lateral surfaces in a fluoroform plasma (Fig. 1.d).

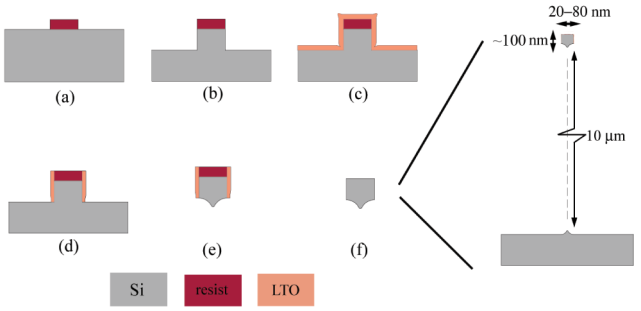

FIGURE 1. Process flow for a single suspended Si NW. This work aims to reach an etch depth of 10 μm while preserving a minimum Si NW width of 20 nm and a thickness of about 100 nm. (a) High-resolution lithography. (b) Anisotropic etching. (c) Conformal coating of low-temperature oxide (LTO). (d) LTO removal from horizontal surfaces. (e) DRIE with adequate undercut to release the Si NW, while not considerably attacking it from its unprotected bottom surface. (f) Removal of protective layers.

A deep reactive ion etching (DRIE) recipe is developed to produce an adequate scallop size allowing the release of Si NW at the end of the first cycle of etching (Fig. 1.e). Further cycles of etching are carried out to obtain a single Si NW over the desired trench depth. Finally, both LTO and HSQ are removed by hydrofluoric acid (HF) vapor etching (Fig. 1.f).

III. RESULTS AND DISCUSSIONS

A. SILICON NANOWIRES

An array of resulting Si NWs is shown in Fig. 2.a. The process flow yields a 10-μm etch depth, a promising achievement as a device thickness of 10 μm is frequently used in all-Si MEMS applications. Opposing triangles represent anchors spanned by Si NWs with widths between 20-80 nm. An aspect ratio (NW length/width) range of 10-150 is achieved leading to Si NW lengths between 200 nm and 12 μm. A process yield above 90% is obtained, indicating high repeatability in a research laboratory and hence suitability for batch fabrication.

Fig. 2.b and 2.c depict a Si NW with the smallest width of 20 nm, and a moderate width of 30 nm, respectively.

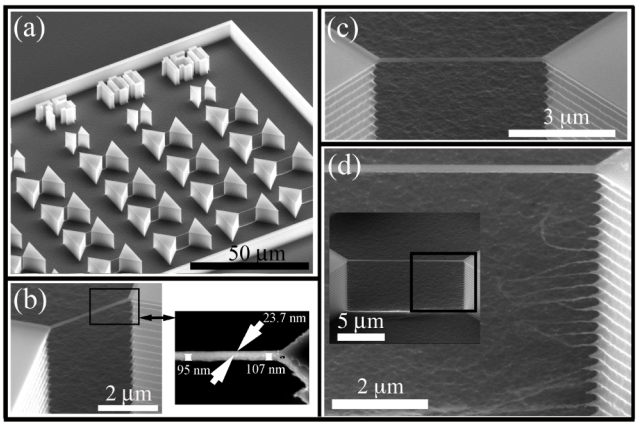

FIGURE 2. (a) An array of Si NWs anchored between two 10-μm-thick, triangular supports. (b) A Si NW with the minimum achievable width of 20 nm (measured as 23.7 nm in a Zeiss Merlin SEM). (c) A Si NW with a moderate width of 30 nm. (d) A Si NW with the maximum width of 80 nm. Remnants of DRIE in the form of discontinuous Si whiskers are visible. Inset indicates their location with respect to the Si NW.

Average Si NW thickness (out-of-plane dimension defined by the first RIE step of Fig. 1.b) is observed to be 100 nm (close-up provided in the inset). The reduction of the original 150 nm thickness related to RIE etch depth (Fig. 1.b) to 100 nm after DRIE (Fig. 1.e) is an indication of isotropic etching of the Si NW over its unprotected bottom surface. The midsection of the Si NW is further thinned down to 95 nm, whereas near the anchors the thickness increases to 107 nm. As etching from the bottom takes place in a mass-transport-limited fashion, Si NW midsection is exposed to a higher isotropic etching rate due to faster diffusion away from the supports. Under the conditions reported above, a thickness uniformity within 10% is obtained. Controlled by the isotropy of the specific etch recipe, achieving such dimensional uniformity in thickness has been more challenging compared to the uniformity in width.

HSQ thickness is observed to be the main limiting factor for the etch depth, as prolonged etching leads to the loss of HSQ. Etch mask thickness or materials can be tailored, if a need for thicker devices, *e.g.* 50-μm-thick SOI, arises. In case of a more resistant etch mask the loss of Si from the unprotected Si NW bottom surface would be critical as explained above. Replacing DRIE with an isotropic release step such as a high-pressure RIE was previously observed to pose significant challenges for Si NW thickness and etch depth [12]. An optimization of the interplay among the initial Si line thickness (Fig. 1.b) and the isotropic etch component of DRIE can be further carried out for a desired combination of Si NW thickness and overall etch depth.

The importance of recipe optimization is further exemplified in Fig 2.d showing a Si NW with the maximum NW width of 80 nm utilized in this study. As the sum of the resist width defined by the lithography of Fig. 1.a and LTO sidewall coating thickness of Fig. 1.d sets the maximum linewidth to be etched for a complete Si NW release, an adequate SF_6 etch cycle duration has to be determined. In this study, discontinuous, residual Si whiskers, remnants

from DRIE of Fig. 1.e, survive for a NW width of 80 nm. For all widths smaller, the undercut associated with DRIE recipe successfully removes Si underneath the Si NW. On the contrary, further reduction of the isotropic etch component will lead to the formation of Si NW arrays as previously observed in the form of Si NW stacks [13].

A further cross-sectional study is carried out by using Focused Ion Beam (FIB) milling. Prior to FIB, Si NWs are coated with a 20-nm-thick Pt layer by atomic layer deposition (ALD) to enhance contrast during scanning electron imaging. 10 Si NWs with widths of 20-40 nm and aspect ratios between 50-150 are studied. Fig. 3.a depicts a 40-nm-wide Si NW with an aspect ratio of 50 cut both at its center and near the anchor. Si NWs exhibit a rectangular cross-section with the maximum thickness at the anchors. Thickness is observed to decrease by 10 % towards the middle, as discussed in Fig. 2.b. The width also increases by 10 % towards anchors due to the backscattering effect in electron beam lithography [14]. The increase of both the width and the thickness from the center (Fig. 3.b) to the anchor (Fig. 3.c) is evident in cross-sectional micrographs. A close-up near the center (Fig. 3.d) reveals a 16-18 nm-thick Pt sheath as well as a rectangular cross-section. This cross-section is different from the scallop profile as depicted in Fig. 1.f. This difference hints at the relatively large size of the scallop radius of curvature compared to the NW width.

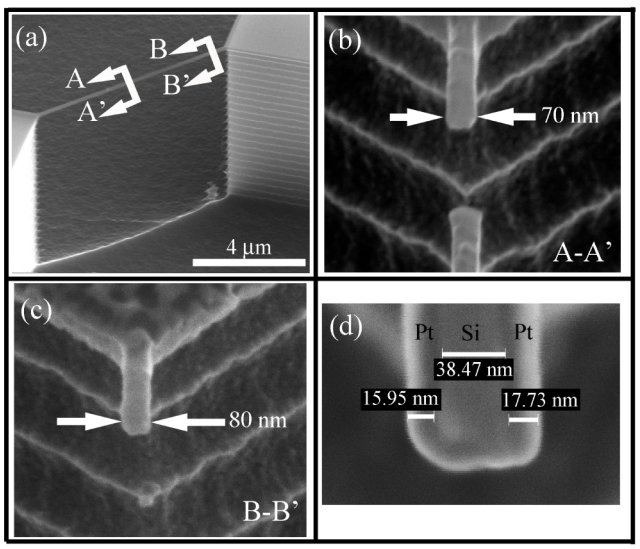

FIGURE 3. (a) A 40-nm-wide Si NW for FIB study. (b) FIB cut near the midsection (A-A') revealing a width of 70 nm including an ALD-coated Pt thickness of about 20 nm. (c) A cross-section near the anchor (B-B') indicating an increase in the NW width. (d) A close-up near the center showing a rectangular Si core enveloped by the Pt film.

B. NANOMECHANICAL CHARACTERIZATION

Resulting structures are tested through bending experiments in an atomic force microscope (AFM) through Bruker Peak Force QNM (Quantitative Nano Mechanical Mapping). A calibration routine is followed for each cantilever and the correction factors are taken into account through the native AFM software for cantilever (Bruker FastScanA tip) stiffness and deflection sensitivity. During subsequent imaging, the AFM tip is positioned in the middle of the Si NW, first in a coarse manner and then more precisely by pursuing the point of maximum deflection upon consecutive zooming.

Imaging is followed by the ramping mode in which force is applied gradually until fracture at 9 μN (Fig. 4.a). Elastic behavior of Si NW is evident, where each loading with increased set-point force overlaps with previous ones. Further tests are performed on 4 Si NWs with a width of 30 nm and a length of 1.5 μm. (Fig. 4.b). The average stiffness exhibits a four-fold increase when compared to the expected value with the bulk modulus of elasticity of 169 GPa taken for <110> Si.

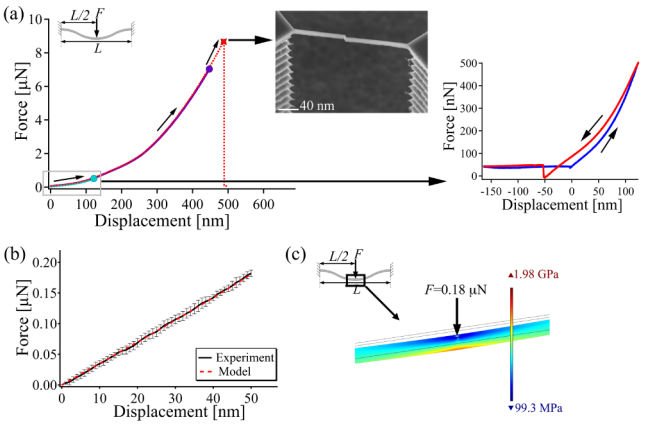

FIGURE 4. (a) Mid-span loading curves to three different set-point forces. Fracture takes place at 9 μN at the point of loading (micrograph in the inset). Hysteresis associated with loading to 0.5 μN and unloading is provided in a separate inset. (b) Loading curve obtained on four Si NWs in the linear regime. (c) Uniaxial stress distribution in Si NW mid-span for 0.18 μN.

Such stiffening is reported for double-clamped NWs, where surface stress is claimed to lead to an increase in the apparent modulus with higher aspect ratios [15]. As surface stresses cannot cause contraction in the double-clamped configuration, a tensile stress develops increasing the flexural stiffness. In addition, fabrication-related defects and intrinsic stresses develop [16]. Recent studies hint at the misinterpretation of the intrinsic stress effect as an increase in the modulus of elasticity [17], [18]. Hence, both the modulus and intrinsic stress have to be extracted from measurements. As no appreciable change in the modulus is predicted for Si at the scale of interest of this work [19]–[21], the stress effect is modeled using finite element analysis with the bulk modulus. The finite element model is based on tetrahedral elements, where an initial stress is incorporated as a domain boundary condition. Experimental stiffness is matched, when this tensile intrinsic stress reaches 850 MPa. As such high intrinsic stresses are common in nanofabrication [21], [22], this study confirms the necessity to incorporate them in nanomechanical models. However, one should exercise caution in the quantification of the intrinsic stress, as dimensional variations, shown to be as much as 10%, and the lack of

modeling of the actual tip shape and tip-sample interactions constitute sources of uncertainty.

As Si NWs and anchors are etched from the same crystal, a high-level of structural integrity is expected. Accordingly, in 14 out of 17 tests, fracture is observed to take place at the point of loading as opposed to the anchors (inset of Fig. 4.a). For 0.18 μN, where the deformation is still linear (Fig. 4.b), the maximum uniaxial stress is found to be already on the order of 2 GPa (Fig. 4.c) surpassing the strength of bulk Si. Using the same finite element model with geometric non-linearity, fracture strength is estimated to exceed previously reported 12 GPa [23].

IV. CONCLUSION

A technique for the monolithic fabrication of Si NWs within 10-μm-thick Si layers is developed. SiNWs as narrow as 20 nm are demonstrated with a maximum aspect ratio of 150. Thickness control is achieved through a combination of Si etch processes. Their mechanical integrity is tested using AFM bending tests. As the Si NW does not remain buried at the bottom of a thick Si layer, one can now pursue a set of surface processes such as doping and contact formation apart from MEMS fabrication. This ability constitutes an advantage for applications, where the integration of Si NWs with thicker MEMS shuttles is of interest.

ACKNOWLEDGMENT

Authors gratefully acknowledge help by CMI Staff.

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