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Self-assembly-based batch fabrication of nickel–iron nanowires by electroplating

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Abstract
The reason behind the majority of difficulties encountered in the integration of nanoscale objects with microelectromechanical systems can almost always be traced back to the lack of batch-compatible fabrication techniques at the nanoscale. On the one hand, self-assembly products do not allow a high level of control on their orientation and numbers, and hence, their attachment to a micro device is problematic. On the other hand, top-down approaches, such as e-beam lithography, are far from satisfying the needs of mass fabrication due to their expensive and serial working principle. To overcome the difficulties in micro–nano integration, a batch-compatible nanowire fabrication technique is presented, which is based on fabricating nanowires using simple lithographic techniques and relying on guided self-assembly. The technique is based on creating cracks with a predetermined number and orientation in a thin SiO_2 coating on Si substrate, and then filling the cracks with an appropriate material of choice. After the SiO_2 coating is removed, nanowires remain on the Si surface as a replica of the crack network. The technique, previously confined to electroless deposition, is now extended to include electroplating, enabling the fabrication of nanowires of various alloys. As an example, arrays of NiFe nanowires are introduced and their magnetic behaviour is verified.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The progress in the field of integration of microelectromechanical systems (MEMS) with nanoscale features such as nanowires has been hampered so far by a lack of batch-compatible fabrication techniques. Nanoscale features are fabricated using either self-assembly-based techniques or top-down methods. Limiting the scope of the discussion to nanowires, available self-assembly techniques can be summarized as follows:

- Filling of porous media such as anodic alumina [1–3], ion track-etched polymers [4] or selectively etched diblock copolymers [5] with a second material using techniques such as electrochemical deposition, chemical vapour deposition or pressure injection;
- Vapour–liquid–solid (VLS) method or derivatives of it, where whisker growth takes place through precipitation at the solid/liquid interface at a supersaturated alloy in the form of a nanodroplet [6–11];
- Coating of biological molecules such as peptides [12] or DNA [13–15] with metal or conductive polymers;
- Step-edge decoration on graphite surfaces [16];

Although these methods are successfully used to fabricate a variety of nanowires, they cannot provide the level of control on the directionality and the number of nanowires required for integration with MEMS. At present, these self-assembly products are integrated with micro structures using one of the following techniques:

(1) Imparting directional growth into self-assembly by using external electrical fields [17] or selective deposition of nucleation sites [18],
(2) Using conventional self-assembly and then removing nanowires from their fabrication sites, such as alumina templates. These nanowires are dispersed in an

appropriate medium, such as isopropyl alcohol. Dispersed wires are then aligned with respect to micro structures using electric [1] or magnetic [19] fields, microfluidic alignment [20], complementary surfaces with appropriate functionalization, for example, using DNA [13, 21, 22] or electrostatic attraction [23] and the Langmuir–Blodgett technique [24, 25] among many other methods. Sometimes amorphous carbon films are used to increase the adhesion between the nano extension and the main structure [26].

In the latter technique, micro structures and nanowires are fabricated separately and nanowires are attached to the micro structure using external fields or secondary forces, whereas in the first technique, the micro structure is fabricated first and nanowires are grown on top of the micro structure. It is clear that none of these solutions provide the required level of order. For example, placing a single nanowire at a particular location on a MEMS that would serve as a robotic arm or a manipulation tool is out of the scope of these techniques.

On the other extreme, of course, are the top-down methods which are used more frequently than self-assembly techniques due to the obvious reasons of perfect control on directionality and number of nanowires. Electron-beam lithography [27, 28], direct growth of nano extensions on MEMS using focused-ion-beam chemical vapour deposition [29] or electron-beam deposition [30, 31] are most widely used micro–nano integration techniques. Etching micron-level structures down to the nanoscale using focused ion beam is also reported [32]. However, no matter how precise the end-product turns out to be, the need to eliminate serial processes from the fabrication flow is crucial for mass production. It is clear that the ideal technique for micro–nano integration would involve a self-assembly-based bottom-up process for nanofabrication that is, at the same time, compatible with the philosophy of batch fabrication. On the one hand, this enables the fabrication of microscale features along with their interfaces with the macro world using well-known techniques such as photolithography and wire bonding, and on the other hand, an appropriately designed self-assembly method will realize the growth of nanoscale features on the micro device. In this way, a marriage between MEMS and nanofabrication can be accomplished within the boundaries of batch fabrication.

In this study, we present the results of a fabrication technique that is based on fabricating nanowires using simple lithographic techniques and relying on guided self-assembly. The technique relies on creating crack networks in a thin coating on Si, where the number and direction of cracks are predetermined. The cracks then serve as moulds to be filled with a second material. In principle, this technique is similar to SNAP, where, instead of cracks, selective etching of a superlattice results in a mould for parallel nanowires with a chosen periodicity [33, 34].

The fact that a variety of materials can be used, including NiFe, imparts a second aspect to the implications of the study in addition to facilitating micro–nano integration: made of a magnetic alloy, oriented nanowires themselves can be used as actuators and sensors when placed in an external magnetic field. Verification of the magnetic behaviour of NiFe nanowires will be given at the end of the paper after the fabrication technique is discussed and examples of resulting nanowire networks are presented.

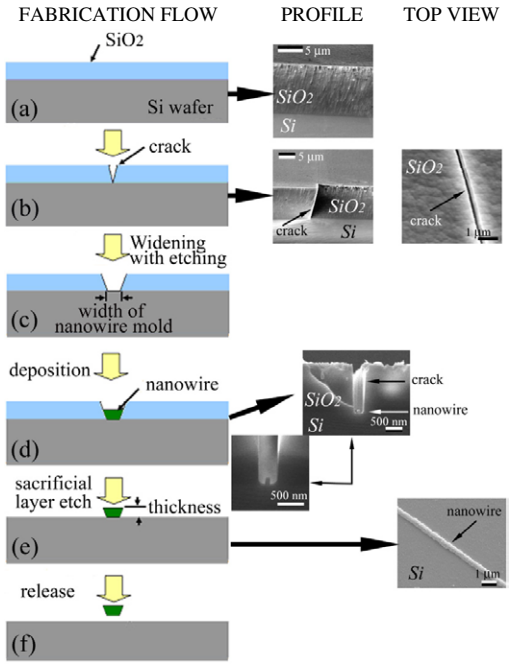

Figure 1. Fabrication process of nanowires and micrographs of resulting structures at each step: (a) deposition of a 5 μm-thick oxide layer; (b) formation of cracks by heat treatment; (c) HF etch of the cracks to obtain a wider and oxide-free plating base; (d) electroplating of NiFe in the nano moulds; (e) oxide strip by HF etch; (f) KOH etch for final release of the devices. Note: scanning electron micrographs are added for descriptive purposes. They do not necessarily belong to the same batch.

2. Experimental method

The fabrication technique based on electroplating is illustrated in figure 1. A thin sacrificial layer is deposited on Si substrate, which develops tensile stresses upon appropriate heat treatment. When tensile stresses are high enough, they lead to fracture in the thin film. These cracks are then filled with a second material. When the sacrificial layer is removed, a replica of the crack network is obtained.

This crack network would be of little use if the location of cracks and their orientation cannot be determined *a priori*. It is indeed observed that in the absence of any intervention, cracks follow the ⟨100⟩ orientation of the underlying Si wafer, as shown in figure 2 for a plasma-enhanced chemical vapour deposited (PECVD) SiO_2 film, and their location and number are completely random. Similar behaviour is also observed for other films on Si, including xerogel silica [35]. As a consequence, a successful integration with MEMS cannot be realized as is the case with similar fracture studies [36].

Therefore, when the method was first introduced [37], it was emphasized that crack paths can indeed be dictated by etching (i) sharp corners as crack initiation sites and (ii) free edges in the form of deep trenches for crack attraction sites within Si, prior to sacrificial layer deposition, as seen in figure 2. This patterning can be carried out by conventional photolithography. Upon sacrificial layer deposition and thermal treatment, a network of nanoscale cracks evolves guided by stress distribution due to this simple, microscale

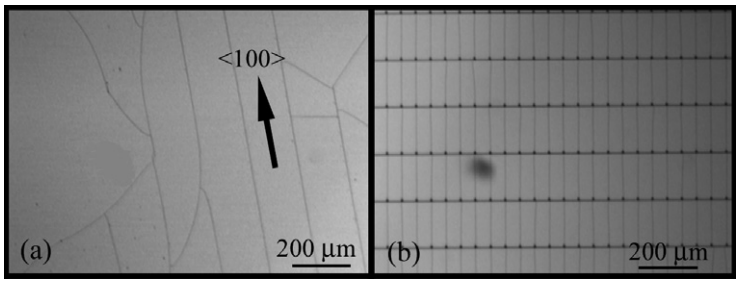

Figure 2. Effect of patterning. (a) Micrograph showing an unpatterned sample where the crack network is highly influenced by the anisotropy of the underlying substrate. Cracks in SiO_2 follow the ⟨100⟩ orientation of the Si substrate. Si, having the minimum stiffness along this direction, allows cracks to maximize their widths, and thereby release the maximum amount of energy in the strained structure. (b) Micrograph showing the crack network of a patterned sample at the same magnification, where a high level of control on both the direction and number of cracks is visible. Cracks initiate at sharp corners and terminate at free edges both etched in Si prior to SiO_2 deposition.

patterning. The number and orientation of etched corners and trenches determine the final distribution of cracks.

The surface density of nanowires is limited by stress effects. First, if two cracks are brought too close to each other, the stress states around them will be disturbed due to the existence of the neighbouring crack, and as a result, they will divert from their original paths. The 50 μm distance between cracks in figure 2(b) is sufficient to screen cracks from this effect. In our studies, we observed that reducing crack spacing from 50 μm down to 25 μm does not divert cracks within the first 30 μm of their trajectory, after which secondary cracks take a turn and meet already existing cracks perpendicularly.

The second aspect, regarding the density of nanowires is concerned with the question of how close a crack can be initiated next to an existing one where the energy of the strained medium is already released. Apart from keeping the straight trajectory, this aspect is concerned with the fundamental limitations, which is not studied further here. It is to be noted that for integration purposes with MEMS, the length scale in the first aspect (25–50 μm) is satisfactory. The fundamental limit would be of interest if one tries to fabricate a diffraction grating or a nanomechanical resonator with this technique.

In this study, Si in the form of 4 in-diameter, 500–550 μm-thick, n-doped, 0.1–0.5 Ω cm resistivity ⟨100⟩ wafers is used as the substrate. The patterns of crack initiators and terminators are etched to a depth of 10 μm using inductively-coupled plasma deep reactive ion etching (ICP-DRIE). SiO_2 deposited using the PECVD technique is chosen as the sacrificial layer due to the ease of altering SiO_2 chemistry and the reasonably well understood mechanism of tensile stress generation [38] and fracture [39]. Deposition conditions of silicon dioxide are reported elsewhere [37]. Heat treatment is carried out at 400 °C for 20 min under nitrogen flow. The occurrence of cracking is observed to be almost 100%, i.e. each crack initiator is observed to lead to cracking. As a novelty, electroplating without any seed layer is introduced for filling cracks as opposed to electroless Ni deposition that was used previously [37]. This improvement enables the fabrication of nanowires of various alloys, such as NiFe, where magnetic properties can be controlled by changing deposition parameters, which again is not possible with electroless deposition. The sacrificial SiO_2 layer also serves as a natural mask for electrodeposition without raising the need for subsequent lift-off.

After annealing, cracks are observed to initiate at sharp corners terminating at free edges. From a process optimization point of view, the sharpness of the corners of the crack initiation sites is an important issue for the success of the technique. For this purpose, a high-power RIE recipe is necessary in order to achieve anisotropic etching and eliminate round corners. In addition to the RIE parameters, the sharpness can also be retained by using a thinner resist because it helps both in exposure and development processes. However, it should be kept thick enough to survive the RIE process. On the other hand, as the thickness of the sacrificial oxide layer increases, tensile stresses induced due to annealing also increase and crack initiation is facilitated further [40]. If oxide thickness exceeds the depth of the crack initiation sites, no cracking will be observed. The effect of the depth of crack initiation sites is not studied further and it is kept constant at 10 μm.

After cracking, back side of the wafer is masked by a 0.2 μm-thick blanket resist layer to prevent deposition of a NiFe permalloy film on this side. Since the width of the cracks is on the order of a few nanometers at the SiO_2/Si interface, the cracks are widened to a desired dimension by wet etching in hydrofluoric acid (HF) just before electroplating. Etching also helps create an oxide-free plating base for the deposition step. Electrodeposition is performed using a standard permalloy bath [41]. Saccharine is added to the electrolyte to reduce residual stress which may lead to buckling of the nanowires. During deposition Si walls of etched patterns are also covered with NiFe, acting as anchors for the nanowires. After deposition, the remaining oxide layer is completely removed by wet etching in HF. Finally, the nanowires are released by KOH etching of the Si from underneath.

3. Nanowire networks

Figure 3 shows scanning electron microscopy images of the resulting nanowire network and single nanowires before being released. Nanowires are well aligned following the original crack pattern shown in figure 2. They are 250 μm long, and they have a periodicity of 50 μm. Figure 4 shows the atomic force microscopy results of the same network. The heights of

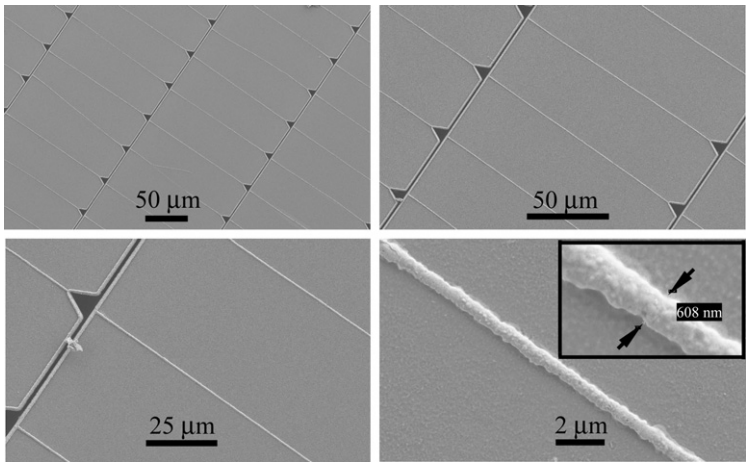

Figure 3. Scanning electron micrographs of NiFe nanowire networks with close-up views of single nanowires. The crack network of figure 2 is replicated here with metallic lines. 10 μm-deep, ICP-DRI etched triangular crack initiators and crack terminators, in the form of deep trenches, are visible.

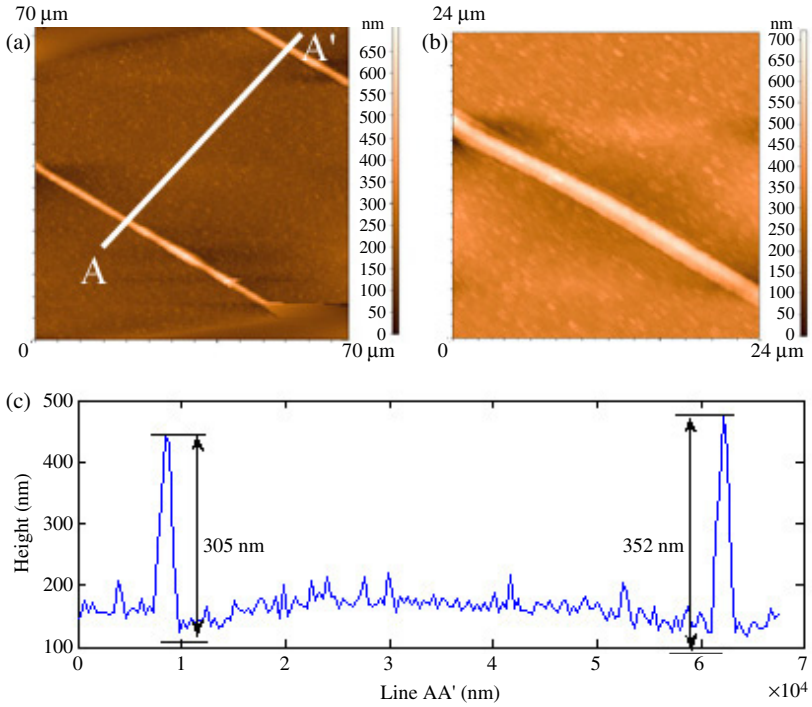

Figure 4. (a) AFM image of two nanowires. (b) Blow-out view of the nanowire on the left. (c) Surface profile along the line AA′.

both nanowires in the figure are of the order of 300 nm as a result of a 1 min deposition.

Nanowires with widths down to 100 nm were previously fabricated with this method using electroless deposition [37]. The width of the nanowires is, of course, determined by the width of the nanowire mould, i.e. the amount of the exposed silicon surface at the crack bottom, and the width of the oxide mould opening at the top. These dimensions depend on the amount of wet etching of the sacrificial oxide layer carried out before the electroplating step. On the other hand, the fundamental limitation of the process is related to the question of how small an opening can be filled with a crystalline material. Depending on the size of the opening and the type of material, there is a critical length scale beyond which the normal nucleation and diffusion process for crystal formation is interrupted, and discontinuities appear along the nanowires. This critical size is measured to be 7 nm for electroplated gold [42]. It should be possible to reach similar dimensions with cracking, as demonstrated by a nanowire growth study in cracks in Teflon-AF films on graphite [36].

Similarly, the thickness variation exhibited by AFM measurements in figure 4 is not related to any fundamental phenomenon, but to experimental limitations and details of the electroplating process. As all deposition work is carried out at chip level, sample dimensions barely exceeded 4 mm by 4 mm, and electrical contact was established at one spot

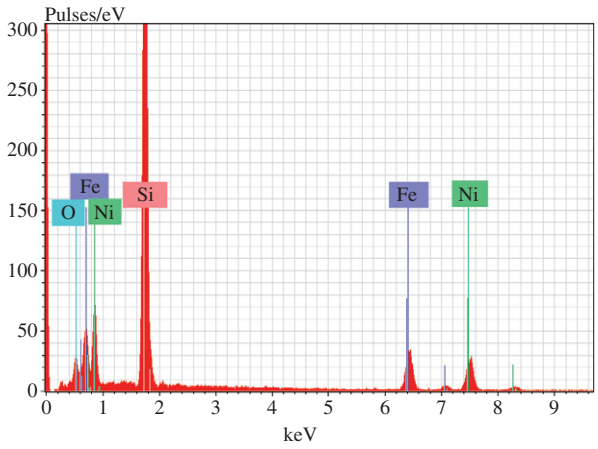

Figure 5. EDS point analysis of a nanowire showing elements existing in the structural material. Si and O are due to the surrounding sacrificial layer and the substrate.

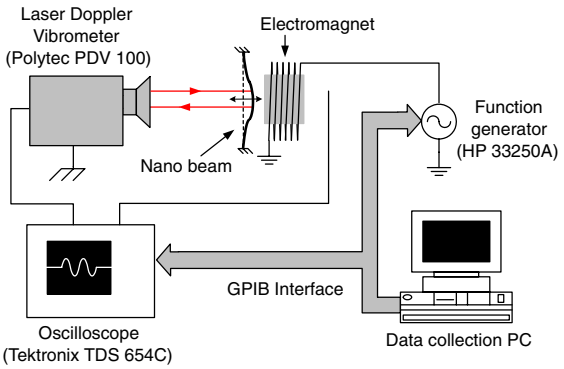

Figure 6. Mechanical characterization setup. The deflections of nanowires under an external magnetic field are picked up by a laser Doppler vibrometer (LDV). A laser spot size of 30 μm ensures that deflection data is collected from a single nanowire.

only. Under these conditions, obtaining a uniform electric field over the entire chip is very difficult. A possible solution to enhance the uniformity of nanowire thickness would involve working at wafer level with multiple contact points, and using a current thief, i.e. an extra dummy cathode for obtaining a uniform electric field near the edges.

EDS results in figure 5 indicate that the atomic Ni/Fe ratio for the nanowires is about 3 at a current density of 40 mA cm^{-2}. Before we proceed with KOH release and measurement of the resulting magnetic behaviour of nanowires, let us mention that the optimization of plating parameters is important for tailoring the constitution of the nanowire material. To reach optimum plating conditions, an exact calculation of the exposed Si area should be carried out in addition to using a current thief. The Si area to be calculated includes the side walls of crack initiation sites in addition to Si exposed at the bottom of cracks. This way the required current corresponding to the ideal current density can be determined. The relation between deposition parameters and the resulting magnetic behaviour is left for further study.

4. Characterization of nanowires

Mechanical behaviour of the nanowires is characterized through a clamped–clamped (CC) nanobeam, which is actuated using an electro coil. Vibration of the beam is detected by a laser Doppler vibrometer (LDV). The LDV can measure the velocity of the point where the laser beam is focused, and it has a minimum laser spot size of 30 μm, which allows one to focus on a single nanowire. The electro-coil induces a magneto motive force (mmf) on the device, and as the structural material of the nanowire is magnetic, the mmf is translated into a magneto static force. This magneto static force is used to deflect the nanobeam in the out-of-plane direction. The magneto static force is proportional to the product of the mmf (and therefore the magnetic field), the magnetization of

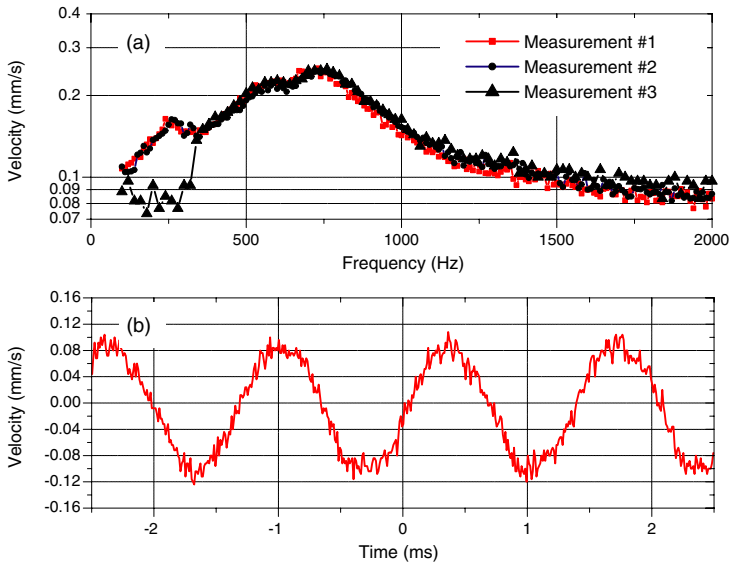

Figure 7. LDV characterization results of a clamped–clamped nanobeam (a) Force-to-velocity transfer function of the device with a frequency varying magnetostatic actuation. (b) Velocity response of the device to a magnetostatic excitation force at 740 Hz.

the permalloy, and the volume of the nanobeam [43]. When the frequency of the magneto motive force is in vicinity of the pass-band of the resonance peak, mechanical quality-factor-amplified vibrations are observed.

Figure 6 shows the details of the experimental setup used for the mechanical characterization of the device. A function generator driven electro-coil excites the nanobeam by inducing a frequency-dependent magneto static force. Both the function generator and oscilloscope are controlled by a custom computer program through a general purpose interface bus (GPIB, IEEE 488) communication interface. Figure 7(a) shows the mechanical transfer function of the beam, where three different measurements are plotted in the same graph. The transfer function relates the velocity of the nanobeam to the excitation force, and can be approximated to the response of a second-order band-pass filter transfer function. The average peak-to-peak displacement of the nanobeam at the fundamental resonance is measured as 50 nm. Figure 7(b) is a typical time response of the single CC nanobeam to a sinusoidal electromagnetic excitation force at 740 Hz. Due to the tiny width of the nanobeam (∼600 nm), only a fraction of the laser spot (0.6 μm × 30 μm out of the circular spot with a diameter of 30 μm) is used to obtain the signal, which leads to measurement noise in the sinusoidal response.

5. Conclusion

Using the example of nanowires, it is shown that batch-compatible fabrication for nanoscale objects is possible with serious consequences regarding the progress in the integration of microelectromechanical systems with nanoscale extensions. The technique eliminates the drawbacks of both self-assembly-based and top-down approaches by using simple lithography and guided self-assembly in the fabrication of nanowires, which allows one to decide the number and orientation of nanowires on the chip. Furthermore, the fact that the technique is based on electroplating facilitates the use of various alloys in nanowire fabrication with the possibility of tailoring their constitution for property optimization. The technique is demonstrated with NiFe as the nanowire material, and the resulting magnetic behaviour is verified by actuating free-standing nanowires.

Acknowledgments

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